REMARKS

By this Amendment, Applicants amend claims 1-4, 8 and 11. Claims 1-16 are pending in this application. In the final Office Action of July 7, 2004[1] ("OA"), claims 1-16 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,805,861 to *Gilbert et al.* ("*Gilbert*").

Applicants traverse the rejection of claims 1-16 because *Gilbert* does not anticipate these claims. In order to properly anticipate Applicants' claimed invention under 35 U.S.C. § 102, each and every element of the claim at issue must be found, either expressly described or under principles of inherency, in a single prior art reference. Further, "[t]he identical invention must be shown in as complete detail as is contained in the . . . claim[s]." *See* M.P.E.P. § 2131. Finally, "[t]he elements must be arranged as required by the claim." *Id.*

Independent claim 1, as currently presented, recites a combination of elements including:

> a logic verification unit configured to perform a logic verification . . .
>
> a circuit changing unit configured to change the circuit description after the logic verification and to generate a changed circuit description;
>
> a logic cone specifying unit configured to specify changed logic cones of the changed circuit description based on a result of a formal verification . . .
>
> wherein the logic verification unit performs a logic verification of the changed circuit description using the test vectors related to the changed logic cones.

[1] The Office Action contains a number of statements reflecting characterizations of the related art and the claims. Regardless of whether or not any such statement is identified herein, Applicants decline to automatically subscribe to any statement or characterization in the Office Action.

Gilbert fails to disclose at least the claimed "circuit changing unit." *Gilbert* is directed to "maintaining consistency of logical component and net names used in EDA [electronic design automation] synthesis and logic optimizing tools during the . . . design process" (col. 1, lines 8-13). Although, as the Examiner notes, *Gilbert* mentions "new and old" design versions (col. 9, lines 63-65; see Fig. 4), *Gilbert* does not teach "a circuit changing unit configured to change the circuit description after the logic verification and to generate a changed circuit description," as recited in claim 1.

Gilbert also fails to disclose the "logic cone specifying unit" recited in claim 1. The Examiner notes (OA at 3) *Gilbert*'s disclosure of reading a new design version from a database (Fig. 4, item 44; col. 9, lines 62-63) and selecting "a common cone of logic from both" the new and previous design versions (Fig. 4, item 48; col. 9, lines 2-5). This disclosure in *Gilbert* does not teach a "logic cone specifying unit configured to specify changed logic cones of the changed circuit description based on a result of a formal verification," as claimed. Indeed, *Gilbert* fails to disclose the claimed "logic cone specifying unit."

In addition, *Gilbert* fails to disclose the "logic verification unit" recited in claim 1. The Examiner notes (OA at 2) *Gilbert*'s disclosure of reading "new and old" design versions (Fig. 4, items 42-44; col. 9, lines 63-65), comparing a new cone of logic to an old cone of logic (Fig. 4, item 50), and, based on that comparison, transferring and assigning "component and net names" from the old version to the new version (Fig. 4, items 54, 58, 60). Neither this disclosure nor any other disclosure in *Gilbert* teaches a "logic verification unit [that] performs a logic verification of the changed circuit description using the test vectors related to the changed logic cones," as recited in claim 1.

Because *Gilbert* does not teach or suggest each and every element of claim 1, as a matter of law, it cannot anticipate this claim. As such, the rejection of claim 1 under 35 U.S.C. §102(b) based on *Gilbert* should be withdrawn.

Independent claims 3 and 8, although of different scope, include elements comparable to those of claim 1 discussed above. In particular, claim 3 recites, *inter alia*:

> changing the circuit description after the logic verification;
>
> generating a changed circuit description;
>
> specifying changed logic cones of the changed circuit description based on a result of a formal verification . . . and
>
> performing a logic verification of the changed circuit description using the test vectors related to the changed logic cones.

Likewise, claim 8 recites, *inter alia*:

> instructions configured to change the circuit description after the logic verification and to generate a changed circuit description;
>
> instructions configured to specify changed logic cones of the changed circuit description based on a result of a formal verification . . . and
>
> instructions configured to perform a logic verification of the changed circuit description using the test vectors related to the changed logic cones.

For at least reasons similar to those presented above in connection with claim 1, independent claims 3 and 8 are not anticipated by *Gilbert*.

Because independent claims 1, 3 and 8 are not anticipated by *Gilbert*, the rejection of these claims under 35 U.S.C. § 102(b) based on *Gilbert* should be withdrawn. The rejection of claims 2, 4-7 and 9-16 should be withdrawn as well, at least because those claims depend upon base claims 1, 3 and 8. Applicants thus request withdrawal of the rejection of claims 9-16 under 35 U.S.C. § 102(b) and the timely allowance of those pending claims.

Conclusion

The claimed invention is neither anticipated nor rendered obvious in view of the references cited against this application. Applicants request the Examiner's reconsideration of the application in view of the foregoing, and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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